

MOS FIELD EFFECT TRANSISTOR μ PA1850

PACKAGE DRAWING (Unit: mm)

1.2 MAX.

1.0±0.05

0.1±0.05

0.25

 $-0.6^{+0.15}_{-0.1}$

□ 0.1

:Drain1

:Gate1

:Gate2

2, 3 :Source1

6, 7 :Source2 :Drain2

4

5

0.65 0.8 MAX

 $-0.27^{+0.03}_{-0.08}$ \oplus 0.10 \bigcirc

P-CHANNEL MOS FIELD EFFECT TRANSISTOR **FOR SWITCHING**

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DESCRIPTION

The μ PA1850 is a switching device which can be driven directly by a 2.5-V power source.

The μ PA1850 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

- Can be driven by a 2.5-V power source
- · Low on-state resistance

RDS(on)1 = 115 m Ω MAX. (VGS = -4.5 V, ID = -1.5 A) $R_{DS(on)2} = 130 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.0 \text{ V, Ip} = -1.5 \text{ A)}$ $R_{DS(on)3} = 200 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -2.5 \text{ V, Ip} = -1.5 \text{ A)}$

Built-in G-S protection diode against ESD

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1850GR-9JG	Power TSSOP8

6.4 ± 0.2 3.15 ±0.15 4.4 ± 0.1 3.0 ± 0.1 1.0 ±0.2 $|45\pm0.055|$

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage	VDSS	-12	V
Gate to Source Voltage	Vgss	-10/+5	V
Drain Current (DC)	I _{D(DC)}	∓2.5	Α
Drain Current (pulse) Note1	D(pulse)	∓10	Α
Total Power Dissipation Note2	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

2. Mounted on ceramic substrate of 5000 mm² x 1.1 mm

Drain1 Drain2 Body Body Diode Diode Gate1 Gate2 Gate Gate Protection Protection

Diode

Source1

Diode

EQUIVALENT CIRCUIT

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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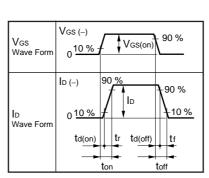
Source2



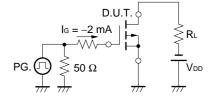
ELECTRICAL CHARACTERISTICS (TA = 25 °C)

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Drain Cut-off Current	IDSS	V _{DS} = -12 V, V _{GS} = 0 V			-10	μΑ
	Gate Leakage Current	lgss	Vgs = ∓ 10 V, Vps = 0 V			∓ 10	μΑ
*	Gate to Source Cut-off Voltage	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-0.5	-1.0	-1.5	V
*	Forward Transfer Admittance	yfs	V _{DS} = -10 V, I _D = -1.5 A	2.0	5.0		S
	Drain to Source On-state Resistance	RDS(on)1	Vgs = -4.5 V, lb = -1.5 A		80	115	mΩ
		RDS(on)2	Vgs = -4.0 V, ID = -1.5 A		85	130	mΩ
		RDS(on)3	Vgs = -2.5 V, ID = -1.5 A		127	200	mΩ
	Input Capacitance	Ciss	V _{DS} = -10 V		260		pF
	Output Capacitance	Coss	V _{GS} = 0 V		300		pF
	Reverse Transfer Capacitance	Crss	f = 1 MHz		45		pF
	Turn-on Delay Time	td(on)	V _{DD} = -10 V		120		ns
	Rise Time	tr	lo = −1.5 A		420		ns
	Turn-off Delay Time	td(off)	V _{GS(on)} = -4.0 V		520		ns
	Fall Time	t _f	R _G = 10 Ω		430		ns
	Total Gate Charge	Q _G	V _{DD} = -10 V		12		nC
	Gate to Source Charge	Qgs	lo = -2.5 A		2		nC
	Gate to Drain Charge	QGD	Vgs = -4.0 V		5		nC
	Diode Forward Voltage	V _{F(S-D)}	IF = 2.5 A, VGS = 0 V		0.80		V
*	Reverse Recovery Time	trr	IF = 2.5 A, VGS = 0 V		750		ns
*	Reverse Recovery Charge	Qrr	$di/dt = 10 \text{ A}/\mu\text{s}$		950		nC

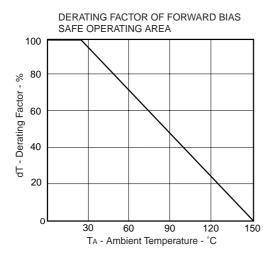
TEST CIRCUIT 1 SWITCHING TIME

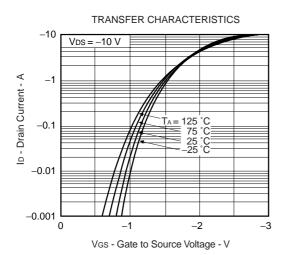


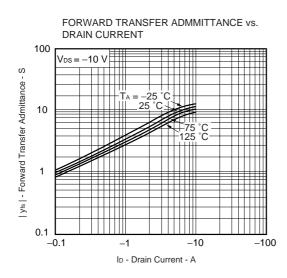
TEST CIRCUIT 2 GATE CHARGE

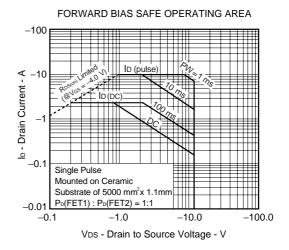


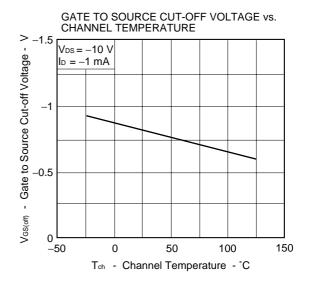
★ TYPICAL CHARACTERISTICS (TA = 25°C)

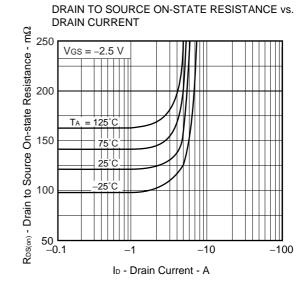






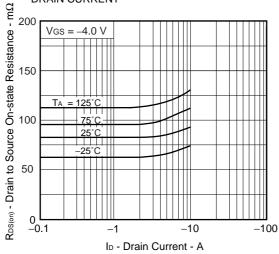




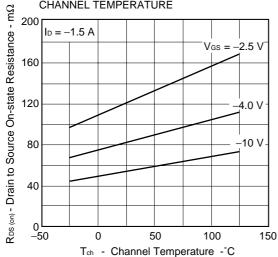


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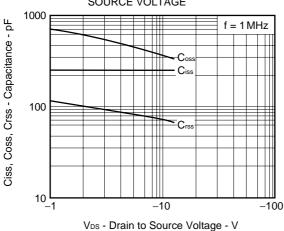
DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



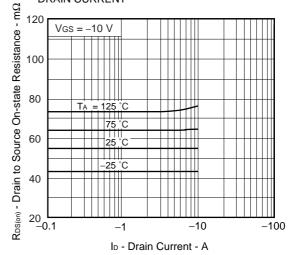
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



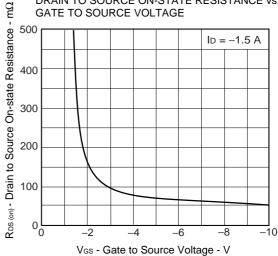
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



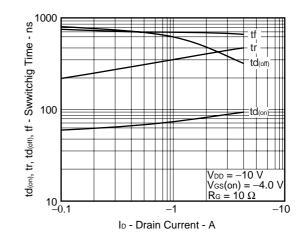
DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**

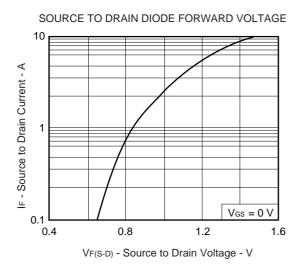


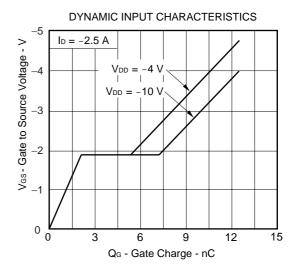
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

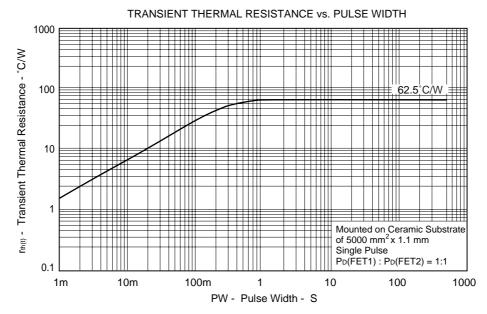


SWITCHING CHARACTERISTICS









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NEC μ PA1850

[MEMO]

NEC μ PA1850

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